REMARKS

Claims 1-50 are pending. In the Office Action dated June 29, 2006, the Examiner took the following action: (1) rejected claims 1-50 under 35 U.S.C. § 101 as claiming the same invention as that of claims 1-50 of co-pending Application No. 11/431,437; (2) objected to claims 19-22 and 32-35 for informalities; (3) rejected claims 1-18, 23-31 and 36-44 under 35 U.S.C. § 112, second paragraph, as failing to distinctly claim the subject matter; (4) rejected claims 1, 3-6, 10-11, 13-15, 19 and 22 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,880,117 to Lin et al. ("Lin"); (5) rejected claims 1, 11 and 19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Published Application No. 2001/0013110 to Pierce et al. ("Pierce"); (6) rejected claims 2, 9, 12, 16-17, 20-21, 23 and 32 under 35 U.S.C. § 103(a) as being unpatentable over Lin; (7) rejected claims 7-8, 24-31 and 33-35 under 35 U.S.C. § 103(a) as being unpatentable over Lin and further in view of U.S. Patent No. 5,621,739 to Sine et al. ("Sine"); and (8) rejected claims 23, 32, 36, 42, 44 and 45 under 35 U.S.C. § 103(a) as being unpatentable over Pierce.

The disclosed embodiments of the invention will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The disclosed invention is a memory module having a plurality of memory devices and a memory hub that is used to access the memory devices, as well as a processor-based system using the memory module and a method carried out by the memory module. The memory hub includes a self-test module coupled to the memory devices. The self-test module couples first and second corresponding signals to at least one of the memory devices. In one of the disclosed examples, the first and second signals are a write data strobe signal and a write data signal. The self-test module further receives output signals from the memory device being tested, and determines based on the received output signals whether the memory device has probably responded to the first and second signals. In one of the disclosed examples, the

received output signals are read data signals. The disclosed self-test module is capable of testing the timing margins of the memory devices because the module is able to alter the relative timing between coupling at least some of the first and second signals to the memory device being tested. Similarly, the self-test module can alter the relative timing between when some of the first signals received from a memory device are used to latch corresponding ones of the second signals coupled from a memory device being tested to evaluate the operation of the memory device. In other embodiments, the memory hub includes a variable frequency clock generator, and the self-test module is able to generate a frequency control signal to alter the frequency of the clock signal during a test of a memory device.

The primary reference cited in the Office Action is the patent to Lin *et al.*, which discloses a memory device testing system 20 including a tester 22 that can be connected to a memory device 26. As shown in Figure 2, the memory device 26 may include a plurality of memory banks 50a-c. The tester 22 applies signals to the memory device 26 to write a pattern of data to the memory device, and it also applies signals to the memory device 26 to read data from the memory device 26. The read data is compared to the write data to determine if the memory device is operating properly. However, the tester 22 is not included in a memory hub, and, fact, is not even part of a memory module that includes the memory device 26. Furthermore, the tester 22 does not alter the timing between signals that it applies to or receives from the memory device 26. Nor does the tester 22 alter the frequency of a clock signal or alter the timing that one signal received from a memory device is used to latch another signal received from the memory device.

According to the Office Action, the Lin *et al.* patent teaches a memory module, but the Office Action does not identify the module by reference numeral or indicate where in the specification a memory module is described. The Office Action also indicates that Lin *et al.* teach a plurality of memory devices ("Figure 2 #50A-c"), but the Lin *et al.* patent describes and shows in Figure 2 a single memory device 26 containing multiple memory banks 50A-C. Multiple memory banks are different from multiple memory devices, each of which can be separately accessed and each of which contain circuitry for processing command and address signals. The Office Action also states that the Lin *et al.* patent teaches altering the relative timing between when some of the corresponding first and second signals in the series are

coupled to the memory device ("Figure 1 #24"). However, reference numeral 24 of Figure 1 is a frequency multiplier circuit that simply generates a CLOCK signal that "is preferably and integer multiple of the frequency of the CLOCK1 signal" that is applied to the input of the frequency multiplier circuit 24. [Column 5, line 34-35]. Nowhere in the Lin *et al.* patent is there any statement or suggestions that the frequency of the CLOCK signal is varied during a test.

The patent publication to Pierce *et al.* describes an on-chip test circuit 11. Therefore, the test circuit 11 is not included in a memory hub as an applicant's disclosed self-test module. Instead, the test circuit 11 is part of a memory device itself that would be connected to a memory hub of the type that contains applicant's disclosed self-test module. During a test mode, the test circuit 11 applies signals to a memory cell array 12 in the memory device chip to cause write data to be stored in the array 12. The test circuit 11 subsequently applies signals to the array 12 to cause read data to be coupled from the memory cell array 12. The test circuit 11 includes an error detection 34 that compares each bit of read data to a corresponding bit of write data to determine if the memory device is operating properly. However, the test circuit 11 does not alter the relative timing between signals that it applies to or receives from the memory cell array 12. Nor does the test circuit 11 alter the frequency of a clock signal used in the memory device containing the memory cell array 12.

The Office Action states that the Pierce *et al.* patent publication discloses a memory module containing "a plurality of synchronous memory devices (Figure 1 #12)...." However, the Pierce *et al.* publication describes and shows in Figure 1 the component identified by reference numeral 12 as a "conventional memory cell array 12." [¶ 13]. It is reference numeral 10 that designates in Figure 1 "portions of a memory device 10 that includes an on-chip test circuit 11." The Office Action also indicates that reference numeral 22 shows a link interface for receiving the memory requests for access to at least one of the memory devices. Reference numeral 22 also purportedly corresponds to a memory device interface through which write memory requests, read memory requests and write data are coupled to memory devices and read data are coupled from the memory device. However, the component designated by reference numeral 22 is neither an interface to a memory device or an interface to a memory access device. Instead, reference numeral 22 designates a test control circuit that receives a test mode signal "TM." The test mode signal TM generates signals that control the operation of the

test circuit 11. The test control circuit 22 is not used for coupling write data to a memory device and read data from a memory device. Instead, a data input buffer 14 and an output buffer 20, respectively, are used for these purposes. The Office Action also states that the Pierce *et al.* patent publication discloses a variable frequency clock generator (" Figure 1 #40") that generates a clock signal that varies over a range during testing. However, reference numeral 40 designates a frequency multiplier circuit 40 that "develops a test clock signal TSTCLK having a frequency greater than the frequency of the external clock signal CLK." [¶ 22]. Pierce *et al.* do not describe the frequency of the test clock signal TSTCLK as being varied in any manner during a test. If the Examiner continues to believe that the frequency multiplier circuit 40 generates a test signal having a variable frequency, he is kindly requested to specify exactly where in the Pierce *et al.* patent publication such is described.

Turning, now, to the claims, claim 1 is directed to a memory module comprising a plurality of memory devices and a memory hub. The memory hub includes, *inter alia*, a self-test module that is operable to couple a series of corresponding first and second signals to at least one memory device in the module. The self-test module is further operable to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the memory device. The self-test module then receives output signals from the memory device, and determines based on the signals whether the memory device properly responded to the first and second signals. As explained above, neither of the cited references disclose a memory hub included in a memory module that alters the relative timing between when first and second signals are applied to a memory device. Claim 1 is therefore novel over the cited references.

The memory module of claim 1 is specified in the context of a processor-based system in claim 23 an therefore patently distinguishes over the cited references for the reasons explained above.

Claim 11 is also directed to a memory module contain a plurality of memory devices and a memory hub. Claim 11 is being amended to more accurately specify the subject matter of applicant's invention. Claim 11 now specifies that the memory hub includes, *inter alia*, a self-test module that receives first and second signals from a memory device and uses the first signals to latch corresponding ones of the second signals. The claim further specifies that

the self-test module is operable to alter over a range the relative timing between when some of the first signals are used to latch the corresponding second signals. The latched second signals are then used to evaluate the operation of the memory device. As explained above, the testing circuits shown in the cited references do not disclose a memory hub that includes any means for altering the relative timing between signals that are received from a memory device. Claim 11 is therefore not anticipated by the cited references.

Claim 19 is directed to a memory module containing a plurality of synchronous memory devices and a memory hub. The memory hub includes, *inter alia*, a variable frequency clock generator that couples to a memory device a clock signal having a frequency corresponding to a frequency control signal. The memory hub also includes a self-test module that generates the frequency control signal to vary the frequency of the clock signal over a range during a test. The self-test module couples a first series of input signals to the memory device. The self-test module then receives output signals from the memory device and uses these output signals to determine whether the memory device properly responded to the series of first signals as the frequency of the clock signal is varied. As explained above, neither of the cited references disclose a memory hub containing any circuitry that alters the frequency of a clock signal applied to a memory device during testing of the memory device. Claim 19 is therefore novel in view of the cited references.

The memory module of claim 19 is specified in the context of a processor-based system in claim 32 an therefore patently distinguishes over the cited references for at least the same reasons that claim 19 is novel in view all of the cited references.

Claim 36 is directed to a method of performing signal timing testing on a memory system having a memory hub coupled to a plurality of memory devices. The method includes generating testing signals in the memory hub that are coupled to the memory devices while the relative timing between the testing signals is varied. Output signals from the memory device that result from the testing signals are generated and coupled to the memory hub. These output signals are then evaluated in the memory hub to determine if the memory devices properly responded to the testing signals. As explained above, the cited references do not disclose or suggest a method of testing a memory device in which the relative timing between signals applied to the memory device is varied. Claim 36 is therefore clearly patentable.

Claim 42 is directed to a method of performing signal timing testing on a memory system having a memory hub coupled to a plurality of memory devices. The method includes generating write data and data strobe signals for each of a plurality of memory operations. The write data are stored in the memory hub and are then coupled to a memory device along with the data strobe signal for each of a plurality of write memory operations. However, the relative timing between the write data and the data strobe signal is altered in at least some of the write memory operations. The write data coupled from the memory hub are stored in the memory devices and subsequently read by coupling read data from the memory devices to the memory hub. The memory hub compares the read data coupled from the memory devices to the write data coupled to the memory devices. As explained above, none of the cited references disclose or suggest a memory hub that alters the relative timing between signals coupled to a memory device, and they certainly do not suggest altering the relative timing between write data and a data strobe signal coupled to a memory device. Claim 42 is therefore not anticipated or obvious in view of the cited references.

Claim 44 is also directed to a method for performing signal timing testing on a memory system having a memory hub coupled to a plurality of memory devices. The method includes generating in the memory hub a memory command and a clock signal for each of a plurality of memory operations. In at least some of the memory operations, the relative timing between coupling the memory command and the clock signal to the memory device is altered. A memory operation is then performed in the memory device for each of the plurality of memory commands. Data are then read from the memory device by coupling read data from the memory devices to a memory hub in each of a plurality of read data operations. The memory hub then uses the read data to determine if the memory devices properly performed the memory operations corresponding to the memory commands. As explained above, the cited references do not disclose or suggest a memory hub that alters the relative timing between signals coupled to a memory device, and they certainly do not suggest altering the relative timing between memory commands and a clock signal coupled to a memory device. Claim 44 is therefore patentable over the cited references.

Claim 45 is directed to a method for performing signal timing testing on a memory system having a memory hub coupled to a plurality of memory devices. The method

includes generating in the memory hub a clock signal having a variable frequency. The clock signal and test signals for each of a plurality of memory operations are then coupled from the memory hub to the memory devices while the frequency of the clock signal is altered for at least some of the memory operations. The memory devices respond to the test signals, and read data stored in the memory devices are coupled to the memory hub during each of a plurality of read operations. The memory hub then uses the read data to determine whether the memory devices properly performed the memory operations corresponding to the test signals. As explained above, none of the cited references disclose or suggest coupling a clock signal and test signals from a memory hub to memory devices while the frequency of the clock signal is altered. Instead, the clock signals generated by all of the prior art devices have a frequency that is fixed during a test.

Applicant is amending claims 19 and 32 to obviate the claim objection noted by the Examiner. Applicant is also amending claims 36, 42 and 44 to correct minor typographical errors. These amendments do not narrow or otherwise alter the scope of these claims.

Applicant requests reconsideration of the Section 112 rejection. The "relative timing" between two signals simply means that the timing of one signal with respect to the timing of the other signal is varied. In this context, there is therefore nothing indefinite about the term "relative timing."

Applicant disagrees with Examiner's comments regarding applicant's duty of disclosure and the prior art cited by applicant. All of the references cited by applicant are references that applicant has reason to believe may possibly be relevant to the claims of this application. As the Examiner may understand, if applicant engages in picking and choosing which of these references to cite, applicant runs the risk of being charged by a potential infringer with intentionally not citing any reference that is argued to be more material than those references chosen to be cited. Although a substantial number of references were cited, applicant believes the number of cited references is substantially less than the number of references that the Examiner would normally review in examining this application. Therefore, the number of cited references is not considered to place an undue burden on the Examiner, although applicant certainly understands the Examiner's desire to avoid reviewing prior art that is not found to be material. Therefore, the prior art cited by the applicant should not be reviewed with any lesser

degree of examination than the prior art in the Examiner's field of search. Finally, applicant does not agree that applicant has a duty to classify the references by their degree of materiality. If the Examiner is aware of any such requirement in 37 CFR or the MPEP, he is kindly requested to point out such requirement. Again, if applicant engages in the practice of classifying the references by their degree of materiality, applicant runs the risk of being charged by a potential infringer with failing to give references argued to be material a sufficiently high rating of materiality for the purpose of misleading the Examiner.

Finally, applicant respectfully request that the obviousness-type double patenting rejection be held in abeyance until a determination is made as to which of the two involved applications will first result in a patent.

All of the claims in the application, *i.e.*, claims 1-50, are clearly allowable. Favorable consideration and a timely Notice of Allowance are therefore earnestly solicited.

Respectfully submitted,

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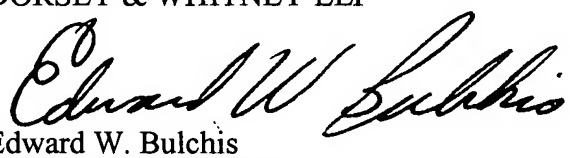

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